ABSTRACT OF THE DISCLOSURE

A method for improved dielectric polish control adjacent to device areas is described. This is particularly important for bipolar structures, although the method may be used for MOS structures as well. The method includes using highly selective methods for removing oxide layers and polish stop layers in a multi-layer film stack, providing an oxide edge step height that is substantially uniform regardless of the size of the adjacent device area. In one embodiment, the multi-film stack includes a first oxide layer, first nitride layer, second oxide layer, and second nitride layer. The multi-film stack is deposited on a substrate. Trenches are then etched through the multi-film stack and into corresponding regions of the substrate. A passivation oxidation layer is grown on the etched trench surfaces. The trenches are filled with oxide for isolating active device regions from one another. A first STI polish is performed, polishing the trench oxide to the level of the second nitride layer, which is then removed. The second oxide layer is then removed. A second STI polish is then performed, polishing the trench oxide to the level of the first nitride layer, which may then be removed. The oxide step height at the edge of each active device region is then approximately equal, regardless of the size of the device region, with a height approximately equal to the thickness of the first nitride layer.